Innovative Packaging Puts Multiple Technologies into a Single Device

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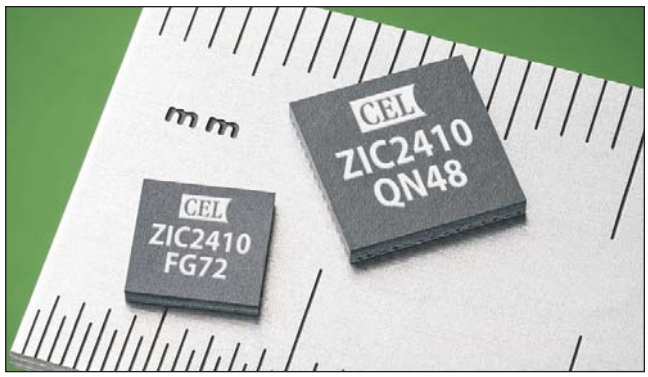
This report is an update on multi-chip packaging technologies, along with notes on the RFICs and ASICs that are the building blocks of new SoC (System-on-Chip) devices. The technique of assembling individual ICs on a semiconductor or insulator substrate instead of a p.c. board is becoming the new standard in components. The resulting single "super component" can be handled like any other component in a production environment, including tape-and-reel delivery and automated assembly.

The other primary advantage of these SoC devices is that they capture specific expertise at the source. In one case, the designers and suppliers of these devices can be highly specialized in the circuitry involved. In the other, they can be packaging experts who handle difficult matters of placing the ICs, then manufacturing and testing the finished SoC modules. In either case, the OEM that is designing a product around the SoC does not need to have the particular expertise in-house.



The ZIC2410 ZigBee transceiver is an example of a SoC device that intergrates multiple functions, inlcuding RF transceiver, power management, microcontroller and other support circuitry.

Package Styles

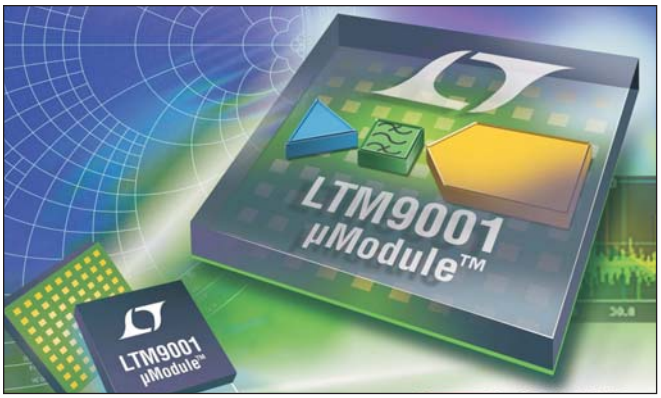
SoC devices offer many of the same package styles as complex single-die ICs: ball grid array (BGA), flip-chip and thin quad flat packages (TQFP). Like any other IC, the package size and number of pins depends on the complexity of the circuit inside, e.g. number of power, control, signal and ground connections required to operate the device.

A wider-view style, usually called System-in-Package (SiP), became popular with oscillators, VCOs and other RF modules, using a nearly conventional ceramic or laminate substrate with solder "lands" or tabs around the edges. A plastic or ceramic cap is used for these devices rather than the IC-like encapsulation of SoC. The SiP approach has evolved to smaller sizes and has adapted the interconnection schemes, resulting in packaging that is similar to SoC.

SoC Substrates and IC Technologies

SoC, as the name implies, uses semiconductor chip fabrication technology on the substrate. For cost purposes, the substrate is most often silicon, with enhancements for improved dielectric properties when necessary for RF circuits. Insulating substrates are also used for higher performance RF devices: thinned silicon-on-insulator (SOI), using glass, sapphire, ceramic or other insulators as the backing material. Conventional high-volume IC processing maintains low cost for the substrate, which includes interconnecting circuitry, coupling and decoupling capacitors, integrated resistors and other supporting passives. Active ICs may be wire-bonded like earlier technology modules, or they may use BGA or flip-chip techniques for more direct (less inductance) attachment to the substrate. The individual ICs may be fabricated in silicon, silicon-germanium, GaAs, or other processes. However, the process must maintain thermal expansion properties that are very close to that of the substrate material.

SiP, as noted above, uses conventional p.c. board or ceramic material as the substrate. Costs are relatively low, as processing these materials is a mature technology. Assembly is more complex, although the same BGA and flip-chip IC packages used for SoC work just fine with SiP. Due to its similarity to conventional p.c. board or chip-and wire modules, SiP can accommodate a wider range of components.



The LTM9001 µModule SoC from Linear Technology combines a high performance analog-digital converter (ADC) with a driver amplifier, literally "packaging" the company's expertise in ADC signal conditioning.

SiP's primary advantage is its flexibility, while SoC's advantage is its lower cost and typically smaller size. One can consider SiP to be a shrinking of conventional assembly techniques, while SoC is an expansion of semiconductor IC fabrication techniques. SoC has the added advantage of currently being a less expensive solution than most large-scale single-chip solutions.

Highly-Integrated Single-Chip ICs

Although SiP and SoC technologies slowed the effort to achieve true single-chip devices, work continues in this area. The biggest challenges in single-chip wireless communications devices are the currents and temperature rise of the power amplifier, and the compromises required for combining RF and digital functions on the same chip. The well-publicized efforts to develop RFCMOS target the latter issue.

The extra effort to develop a single-chip solution is warranted in cases where the power level is not high, and modest overall circuit complexity that allows the use of a process that bridges the gap between the performance of SiGe and the low cost, high density of CMOS. Most short-range wireless devices, such as keyless entry, garage door openers, wireless weather stations, etc., use single-chip devices. Progress is being made on many other applications.

However, for maximum performance, SoC, SiP, or a two- or three-chip solution using conventional assembly is still preferred over the single-chip option. Currently, it is the case that individual functions have highest performance and lowest overall cost when implemented in the preferred semiconductor process. For example, a wireless handset probably has a CMOS baseband processor, SiGe RF transceiver, and GaAs power amplifier. In the case of the Linear Technology LTM9001 pictured above, the two-chip solution has the added performance benefit of simplifying isolation and reducing crosstalk between the analog amplifier circuit and the digital analog-to-digital converter.